

## **Remarks**

Applicants thank the Examiner for the careful examination of this application and the clear explanation of the rejections.

The amended title conforms to the claimed matter.

The new claims obviate the rejections under 35 USC 102. The new claims "particularly point out and distinctly claim the subject matter the applicant regards as his invention."

New claim 26 defines a processor system.

First processor circuitry has a memory transaction bus, a wait signal input, and status signal inputs.

Second processor circuitry has a memory transaction bus, a wait release signal output, and status signal outputs connected with the status signal inputs.

Memory circuitry has first connections with the memory transaction bus of the first processor separate from second connections with the memory transaction bus of the second processor circuitry.

Wait circuitry has memory transaction bus inputs connected with the memory transaction bus of the first processor circuitry and the first connections. The wait circuitry is free of any connections with the memory

transaction bus of the second processor circuitry. The wait circuitry has a wait signal output connected with the wait signal input, and a wait release signal input connected with the wait release signal output.

In contrast, US 6,169,700 to Luo discloses:

An asynchronous wait state generator circuit and method is included in a dual port device, e.g., in a dual port memory, to allow the use of separate address decoders and simultaneous access to memory locations from asynchronously operating, separate ports. When an address collision is detected between accesses on both ports of a dual port device, a wait state signal is generated for the relevant port having the later attempt to access the same memory or other addressable location. In the unique event wherein both accesses are initiated at precisely the same time, a meta-stable element is used to resolve the condition and to allow access to a prioritized port. The wait state signals output for the relevant port of the dual port device are preferably synchronized with the clock signal of the relevant port. Abstract

The dual port memory 100 importantly includes an asynchronous, simultaneous access wait state generator module 110 to handle the particular situation when both address decoders 102, 104 happen to be accessing the same memory element at precisely the same time. In such a case, a wait signal (i.e., a wait state signal) is generated by the asynchronous, simultaneous access wait state generator module 110 to cause one of the simultaneously, asynchronously accessing processors to halt clocking of its port, or wait, until released by the asynchronous, simultaneous access wait state generator module 110 to continue its access. The wait is essentially invisible to the affected processor, but for enduring a longer memory access cycle for that particular access. column 4, lines 29-42

The Luo patent thus discloses a dual port memory that includes wait state circuitry. The wait state circuitry handles “the particular situation when both address decoders 102, 104 happen to be accessing the same memory element at precisely the same time.”

New claim 26 requires wait circuitry having memory transaction bus inputs connected with the memory transaction bus of the first processor

circuitry and the first connections, being free of any connections with the memory transaction bus of the second processor circuitry, and having a wait signal output connected with the wait signal input of the first processor circuitry, and a wait release signal input connected with the wait release signal output of the second processor circuitry.

New claim 26 distinguishes over the Luo patent with the limitations of first processor circuitry having a memory transaction bus, a wait signal input, and status signal inputs; second processor circuitry having a memory transaction bus, a wait release signal output, and status signal outputs connected with the status signal inputs; memory circuitry having first connections with the memory transaction bus of the first processor separate from second connections with the memory transaction bus of the second processor circuitry; and wait circuitry having memory transaction bus inputs connected with the memory transaction bus of the first processor circuitry and the first connections, being free of any connections with the memory transaction bus of the second processor circuitry, and having a wait signal output connected with the wait signal input, and a wait release signal input connected with the wait release signal output.

Claim 26 stands allowable.

Additional independent claim 30 defines wait circuitry.

First processor interface circuitry has a wait signal output, a processor interrupt output, and memory transaction bus connections.

Second processor interface circuitry has a wait release signal input and is free of any connections with any memory transaction bus of the second processor circuitry.

System interrupt interface circuitry has a system interrupt detect input.

Decode logic circuitry is coupled with the first processor interface circuitry.

Control logic circuitry is coupled with the first processor interface circuitry, the second processor interface circuitry, the system interrupt interface circuitry, and the decode logic circuitry.

The disclosure of the Luo patent depicts in Figure 2 a digital comparator 210 as the circuitry providing the wait state 1 and 2 outputs.

Claim 30 distinguishes over the disclosure of the Luo patent with the limitations of first processor interface circuitry having a wait signal output, a processor interrupt output, and memory transaction bus connections; second processor interface circuitry having a wait release signal input and being free of any connections with any memory transaction bus of the second processor circuitry; system interrupt interface circuitry having a system interrupt detect input; decode logic circuitry coupled with the first processor interface circuitry; and control logic circuitry coupled with the first processor interface circuitry, the second processor interface circuitry, the system interrupt interface circuitry, and the decode logic circuitry.

The depending claims also stand allowable as depending from allowable independent claim 26 and as including, in combination with the limitations of the independent claim, additional distinguishing limitations.

The application is in allowable form and the claims distinguish over the cited references. Applicants respectfully request reconsideration or further examination of this application.

Respectfully Submitted,

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